1 Metallization

1.1 Copper technology

1.1.1 Copper technology

Copper has significant advantages compared to aluminum and thus is a good alternative for ever smaller structures. The metal has a much lower resistance than aluminum and is much more efficient in view of power consumption; beacuse of the needs of smaller and smaller feature sizes, aluminum does not fulfill the electrical requirements any longer. Also the electromigration of copper is much less than of aluminum. A change-over can not be averted.

Copper, however, has the disadvantage that it contamintes alomst everything which gets in contact to it. Therefore areas and equipment on which copper is processed, have to be separated from others. In addition, copper is susceptible for corrosion as well as aluminum and has to be covered with a passivation layer. Another advantage of copper is, that there is no need of tungsten to connect the individual copper layers with each other, and therefore additional process steps are omitted as well as thermal issues at the interface of different materials. One of the biggest disadvantages in semiconductor device fabrication is, that copper can not be structured as easy as aluminum in dry etch processes.

The traditional subtractive process for structuring - as it is used for aluminum and other materials - is done as follows:

- deposition of the layer which has to be structured
- resist deposition, exposure and development
- transfer of the resist mask into the layer beneath via dry etching
- resist removal

- passivation

In copper technology one has to use not a subtractive but an additive method: the so called damascene process.

1.1.2 Damascene process

The damascene process makes use of existent interlayer dielectrics in which the vias and trenches for conduction paths are etched. Subsequent, copper is deposited by CVD, PVD + reflow, or in electrochemical/galvanically processes. Finally, the copper is planished by chemical mechanical polishing (CMP).

The damascene process can be seperated into the single and dual damascene process and the latter can be seperated further into the VFTL (VIA First Trench Last) and the TFVL approach (Trench First VIA Last). In the following, both the TFVL as well as the VFTL process are described.

Dual damascene: Trench First VIA Last:
On top of the wafer (in this example on an existing copper layer) different layers are deposited which act as protection, isolation or passivation layers. As an etch stop and protection against gaseous molecules, silicon nitride (SiN) or silicon carbide (SiC) can be used. As interlayer dielectric (ILD), materials with a low relative static permittivity are used, like silicon dioxide SiO_2. Upon a resist mask is patterned.

1. The wafer is coated with a resist layer which is structured in photolithography (Fig. 1.1).

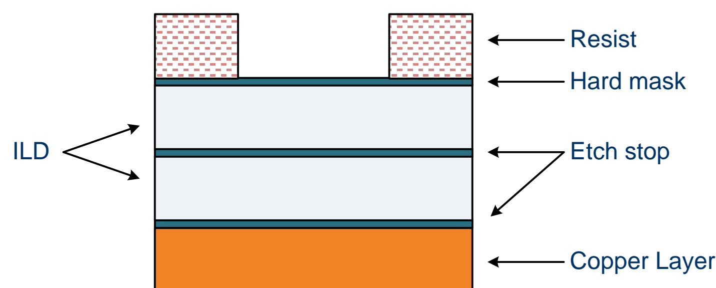

Fig. 1.1: Basic film stack of a damascene approach

2. The hardmask (SiN) and the ILD are etched in a anisotropic dry etch process until the first etch stop layer (SiN) is reached. The resist is removed and the trench for the conduction path is finished. (Fig. 1.2(a)).

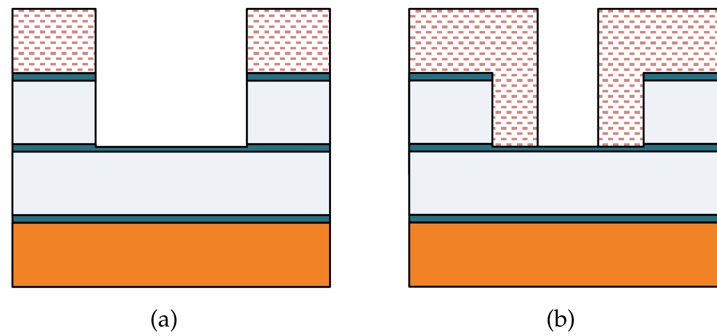

Fig. 1.2: Trench etch and via resist mask

The hardmask on top protects the ILD during the resist ash. This is necessary since the ILD has a similar composition as the resist and therefore is affected by the same process gases. In addition the hardmask acts as a barrier layer during terminal CMP.

3. Next a new resist layer is deposited and structured (Fig. 1.2(b)).

4. Finally the vias are opened in an anisotropic etch process.

With a low energetic etch process, the bottom etch stop is opened to avoid sputtering of the copper beneath which could deposit on the sidewalls and diffuse into the ILD. The resist is removed and a thin layer of tantalum is deposited as a barrier which prevents later deposited copper from diffusing into the ILD (fig. 1.3(a)).

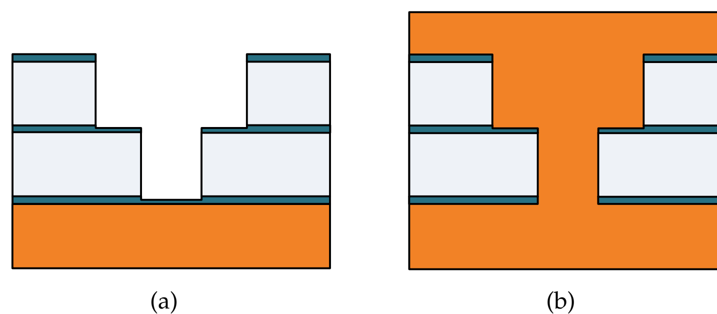

Fig. 1.3: Final structure after etch and copper deposition

5. A thin copper layer acts as a seed layer, so that the vias and trenches can be filled in a galvanically process (Fig. 1.3(b)).

6. The deposited copper is planished in a CMP process (Fig. 1.4).

The big disadvantage of this process is the thick resist layer which is deposited after

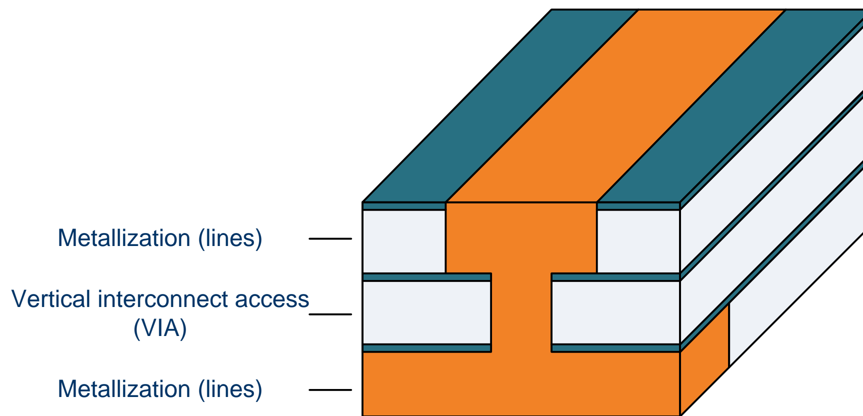

Fig. 1.4: Damascene stack after metallization and CMP

the trenches have been etched (3). To etch the tiny vias in such a thick resist layer is very difficult. For this reason the TFVL approach is done at larger structures only.

Dual damascene: VIA First Trench Last:
The VFTL approach is alike the TFVL process but now the vias are created first.

1. A resist layer to form the vias is structured and the vias transferred into the ILD by an anisotropic etch process till the bottom etch stop layer is reached. To prevent copper from being sputtered out of the metallization beneath, the etch stop must not be opened (Fig. 1.5).

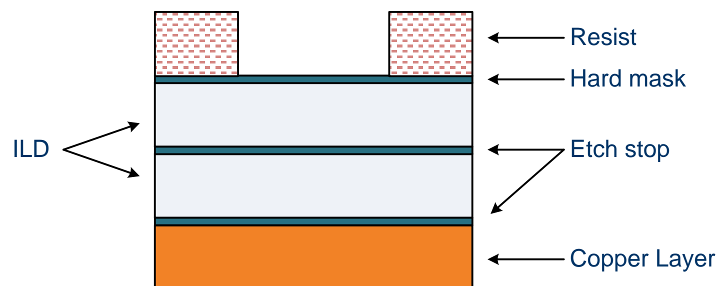

Fig. 1.5: Damascene stack after VIA etch

2. Subsequent the resist is removed, a new resist layer is patterend which represents the trenches; also the previously opened vias are filled with resist (Fig. 1.6(a)).

3. During the trench etch, the bottom etch stop is covered by resist. Next the bottom etch stop is opened in a low energetic process and a tantalum barrier and a copper seed layer are deposited (Fig. 1.6(b)).

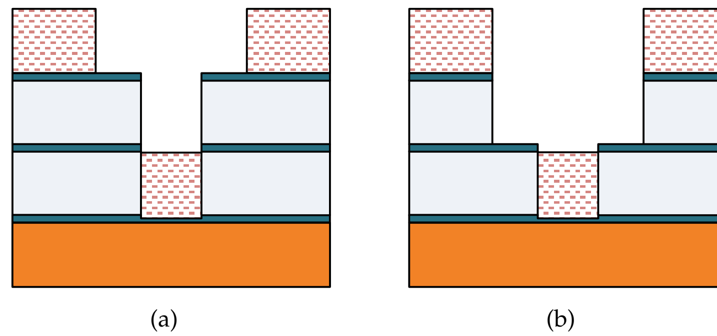

Fig. 1.6: Photolithography and trench etch

4. After the copper deposition, the metal is planished in a CMP process (Fig. 1.7).

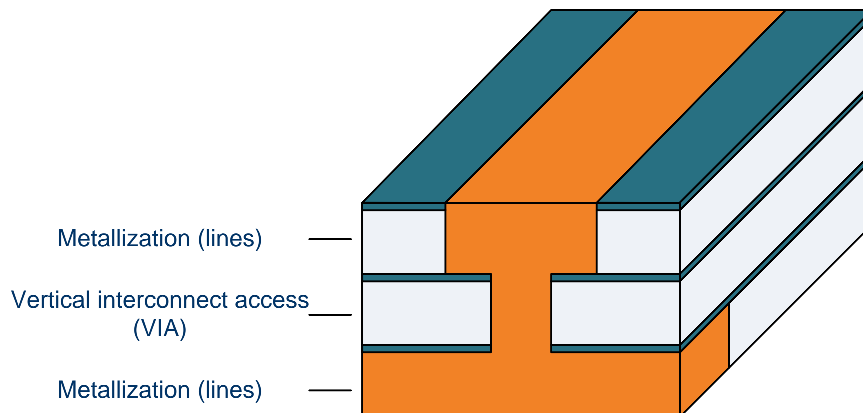

Fig. 1.7: Damascene stack after metallization and CMP

In the single damascene process, the via layer and the trench layer are deposited and structured one after each other, so that there are more process steps needed (ILD deposition ⇒ VIA structuring ⇒ copper deposition ⇒ planarization ⇒ ILD deposition ⇒ trench structuring ⇒ copper deposition ⇒ planarization).

1.1.3 Low-k technology

Since there is a proceeding miniaturization of the structures on microchips to increase packing density, reduce power consumption, and increase switching speeds, the conductors for wiring are moving closer and closer together in vertical and horizontal direction. To isolate the conductors from each other additional films like silicon dioxide SiO_2 have to be deposited as an interlayer dielectric (ILD).

If conductors run parallel or cross each other on different layers upon another, parasitic capacities are created. The conductors represent the electrodes while the SiO_2 in-between is the dielectric.

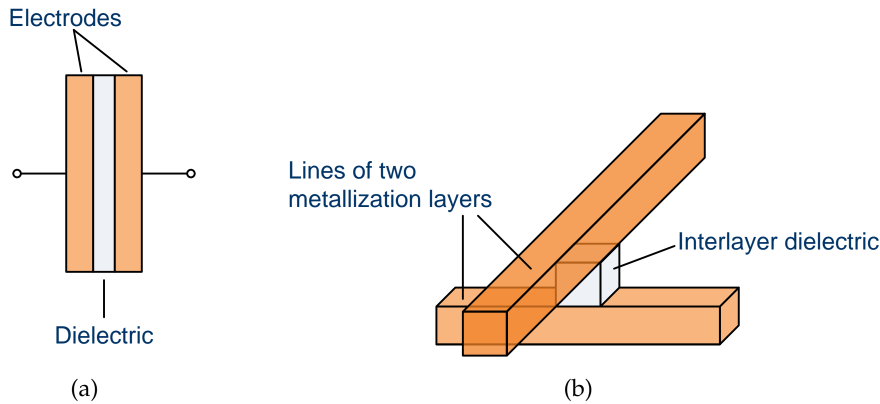

Fig. 1.8: (a) Traditional capacitor and (b) crossing of two conductors

The capacity C is given by:

$$C = \frac{e_0 e_r A}{d}$$

Where d stands for the distance of the electrodes, A is the area of the electrodes, ϵ_0 the vacuum permittivity and ϵ_r (often κ (Kappa) or simplified k) the relative static permittivity of the ILD.

The value of the parasitic capacity influences the electric properties such as the switching speed or the power consumption of a chip, and therefore one tries to decrease C. Theoretical this can be done if ϵ_0, ϵ_r and A are decreased or if d is increased. However, as mentioned above d is getting smaller and smaller, A is preset by electrical requirements and ϵ_0 is a physical constant. Thus the capacity can only be reduced by decreasing ϵ_r.

To sum it up, one needs dielectrics with a $low \epsilon_r$: *low-k*.

The traditional dielectric, SiO_2, has a relative permittivity of about 4. Low-k referes to materials whose ϵ_r is less than that of silicon dioxide. Beyond that there will be Ultra-Low-k materials with an ϵ_r of less than 2.4. The permittivity referes to the polarization (dislocation of charge carriers in the insulator) in the dielectric and is the factor by which the charge of a capacitor is increased relative to vacuum or by which the electric

field inside the capacitor is weakened.

To reduce the permittivity there are basically two possibilities:

- the polarizability of bonds inside the dielectric has to be decreased
- the quantity of bonds has to be reduced by introduction of porosity in the dielectric

The polarizability can be decreased by materials with less polar groups. Candidates are fluorined (FSG, ϵ_r 3.6) or organic (OSG) silicon oxides. However, for smaller and smaller structures this approach isn't sufficient, thus porous films have been introduced. By introduction of porosity there is "empty space" inside the ILD which has - in case of air - a permittivity of about 1, and therefore ϵ_r is reduced for the entire layer. The pores can be introduced by adding polymers which are expelled later by thermal annealing. In case of silicon dioxide one needs about 50 % of pores in the material to achieve a permittivity of 2. If a dielectric is used whose permittivity is 2.5 without porosity, only 22 % pores have to be introduced to achieve a permittivity of 2.

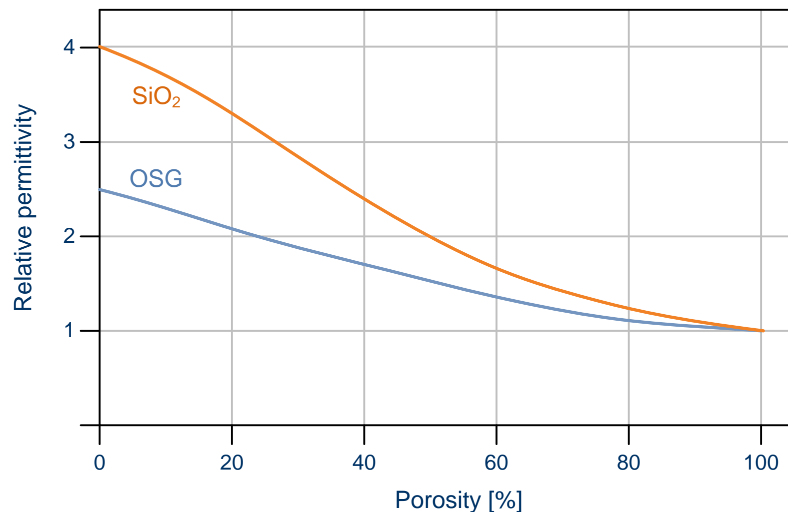

Fig. 1.9: Relative static permittivity against porosity

However, there are several issues to overcome, if one wants to bring in such new materials into semiconductor fabrication.

Due to porosity the density is reduced which results in a lower mechanical resistance. In addition process gases or copper can diffuse into the ILD and cause damage and thus increasing the permittivity or leakage. To counteract this issues, the pores have to

be distributed evenly and must not be in contact with each other. To avoid a diffusion of copper, a thin barrier layer has to be deposited in a seperate process or the pores at the surface have to be closed by ion bombardment.

Like the photoresist used for manufacturing, the organic ILD is composed of hydrocarbon. If the resist is stripped in an ash process, the ILD is affected as well. To avoid this issue, additional layers (like silicon nitride as hardmask) have to be introduced in the film stack.

Chemical formula	**k value**
SiO_2	4,0
$SiO_{1,5}CH_3$	3,0
$SiO(CH_3)_2$	2,7
$SiO_{0,5}(CH_3)_3$	2,55

Tab. 1.1: Overview of organic silicon oxides