Ion Implantation in Semiconductors

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Ion implantation of semiconductors

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Abstract

Ion implantation was first applied to semiconductors over 30 years ago as a means of introducing controllable concentrations of n- and p-type dopants at precise depths below the surface. It is now an indispensable process in the manufacture of integrated circuits. This review gives a brief and selected overview of ion beam modification of semiconductors, treating both fundamental and technological issues of current interest. Damage introduction during ion irradiation and its removal during a thermal annealing step are key issues which are highlighted. Some semiconductors are easily damaged and amorphised (e.g. silicon) whereas others (e.g. gallium nitride) are quite resistant to damage production due to efficient dynamic defect annihilation during implantation. The conditions needed to remove implantation damage also vary dramatically from one semiconductor to another: amorphous layers in silicon can be recrystallised to completely remove disorder at ~600°C, whereas extended defects in gallium nitride require temperatures of >1400°C to remove them. High dose implantation can result in the formation of supersaturated solid solutions, alloys and compounds, often with intriguing properties as a result of the non-equilibrium aspects of ion implantation. Formation of silicon dioxide layers directly during oxygen bombardment of silicon, even under cryogenic implantation conditions, is given as an example. From the standpoint of semiconductor technology, there are several current issues under intense study. Two of these are highlighted with respect to silicon technology: the problems of transient enhanced diffusion of dopants during low temperature annealing due to residual implantation-induced defects, and the need to remove extremely low concentrations of metals from active device regions. Finally, some recent novel applications of implantation in compound semiconductors are treated. © 1998 Published by Elsevier Science S.A. All rights reserved.

Keywords: Ion implantation; Semiconductors; Silicon processing; Radiation damage; Compound semiconductors

1. Introduction

The semiconductor industry has been the juggernaut that has driven implantation technology. There have now been >8000 implantation machines delivered to the semiconductor industry, more than 95% involved in the manufacture of advanced silicon chips alone [1]. Indeed, processing of 0.35 μm CMOS chips can involve more than 30 separate implantation steps [2]. Driven to a very large extent by requirements of the semiconductor industry, there has been an enormous research effort into a broad range of ion beam modification processes in semiconductors over the past 3 decades. For example, the production and removal of implantation damage [3–6], diffusion and electrical (optical) activation of implanted dopants during subsequent annealing [7–10], formation of insulating layers such as silicon dioxide [11] and conducting silicide layers [12] by direct implantation, controlled introduction of irradiation-induced defects to tailor specific electrical [13] and optical [14] properties, together with fundamental studies of defects [15–18] and diffusion [19–21] are all extremely active research areas.

This review briefly treats some of the above areas of research activity, concentrating on damage production and its removal in a range of semiconductors, silicon dioxide formation by oxygen implantation into silicon and a selection of recent technological applications of implantation in both silicon and compound semiconductors. Examples taken from the author's recent research will be given to illustrate each of these areas.

2. Damage accumulation and its removal

When an energetic ion enters a solid it loses energy by two processes: (i) by elastic or nuclear collisions with the matrix atoms causing direct atom displacements and disorder; and (ii) by inelastic or electronic processes in which the electrons of the solid are excited [3]. In

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Table 1
Basic processes during implantation (Si)

Dose (cm^{-2})	Implant concentration	Cascade processes	Structural effects
10^8	Trace (ppb)	Individual tracks	Discrete defects: stable or mobile
10^{12}	Trace (ppm)	Overlapping tracks	Complex clusters, amorphous zones or extended defects
10^{15}	~1 at.%	Complete overlap (~1 dpa)	Dynamic annealing or amorphisation: complex structures
10^{18}	~50 at.%	Composition changes and sputtering	Chemical driving forces: alloying, compound formation and precipitation

semiconductors, only elastic collisions usually generate lattice damage, whereas in insulators, both processes can induce atomic displacements [22]. The collisional or direct displacement processes which occur during the collision cascade take place on a time scale of 10^{-11} s. After such a time the cascade is said to be quenched and, if the discrete defects resulting are immobile and stable, such disorder will be quenched in. However, if defects such as vacancies and interstitials (Frenkel pairs) are mobile at the implantation temperature, then significant dynamic annealing and annihilation of damage can occur during implantation [6]. This dynamic annealing process is much more efficient at normal implantation temperatures in some semiconductors (e.g. gallium nitride) than others such as silicon, as is illustrated later. Indeed, although discrete point defects in silicon are mobile at room temperature [23,24], if the density of defects in the cascade is high (such as for a heavy ion) then discrete defects appear to be efficiently trapped within such damage and implantation damage at room temperature is mostly stable [6]. In such cases, as the dose is increased and the damage from individual tracks overlap, amorphisation can occur. If no annealing of damage occurs during implantation, then amorphisation, or complete disruption of lattice order, should occur at a dose at which each atom has been displaced approximately once (i.e. 1 dpa). At such a dose, $\approx 1 \times 10^{15}$ cm^{-2} for 10 keV Si implanted into Si at liquid nitrogen temperature, for example, the concentration of the implanted ions in the matrix is ~1 at.%. On the other hand, if significant dynamic annealing occurs, amorphisation can be suppressed and the resultant disorder can build up as a dense array of extended defects, particularly dislocation tangles. When dynamic annealing is dominant, the nature of the resultant damage can depend strongly on the implantation temperature (which controls the annealing rates) and dose rate (which controls the rate at which damage is introduced). If a second cascade overlaps the first before the defects from the first cascade have annihilated, then the local defect density is increased and this can stabilise the damage and suppress dynamic annealing. The above features of damage accumulation are reviewed elsewhere [25], but are summarised with regard to implantation in silicon in Table 1 and Fig. 1. In Fig. 1(a), a transmission electron micrograph is shown for implantation of 100 keV. As ions implanted into silicon at room temperature to a dose of 10^{16} cm^{-2} [6]. A continuous amorphous layer is obtained under these conditions. However, in Fig. 1(b) the result of an elevated temperature implantation is shown to give rise to a dense network of extended defects [26].

When dynamic annealing is significant it increases the threshold dose for amorphisation, as shown in Fig. 2 which plots the approximate threshold dose for amorphisation for several (mainly compound) semiconduc-

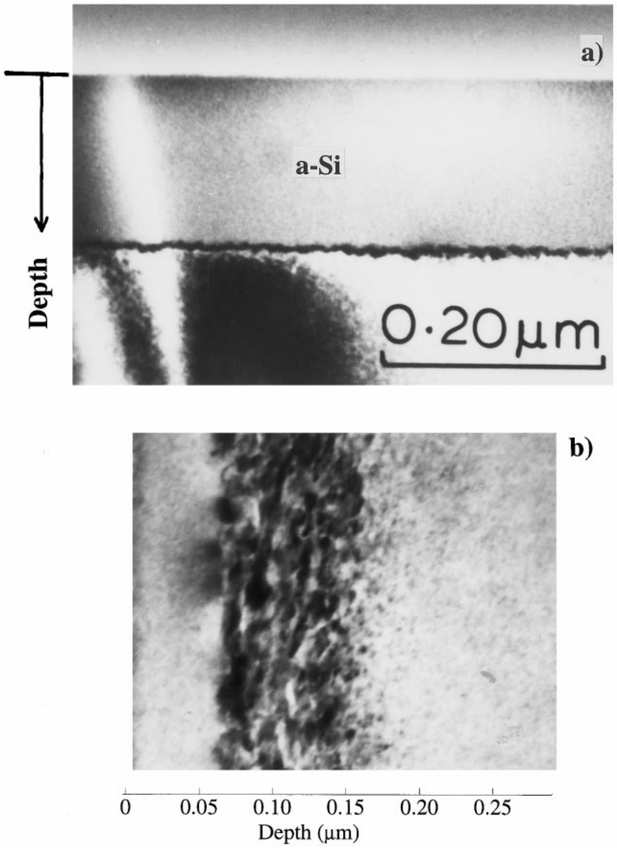

Fig. 1. (a) An XTEM micrograph showing an amorphous layer (a-Si) formed by 100 keV As^+ implanted to a dose of 10^{16} cm^{-2} into Si at room temperature. Note the sharp amorphous–crystalline interface. (b) An XTEM micrograph showing the damage structure from 80 keV Si^+ implant to a dose of 4.4×10^{15} cm^{-2} at 170°C. Taken from [26].

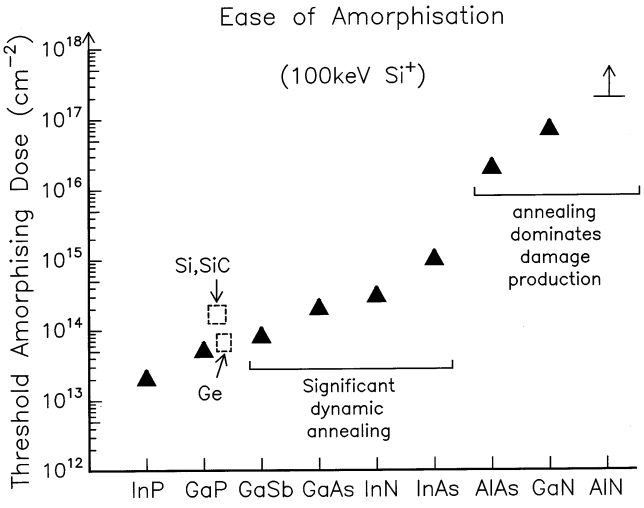

Fig. 2. Estimates of the amorphous threshold dose for various semiconductors normalised for 100 keV Si ion implantation at room temperature at a dose rate of $\sim 5 \times 10^{12}$ cm^{-2} s^{-1}. The data are taken from sources referred to in the text.

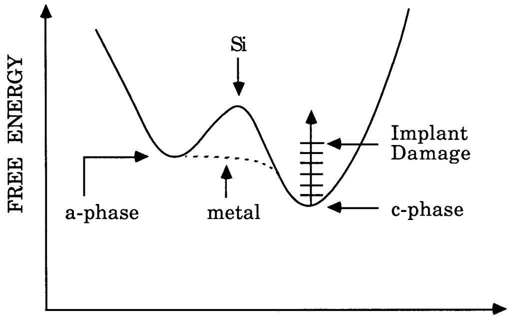

Fig. 4. Schematic representation of free energy differences and barriers between the amorphous and crystalline phases in metals and semiconductors. Taken from [25].

tors. This plot uses 100 keV Si^+ ions at a dose rate of $\sim 5 \times 10^{12}$ ions cm^{-2} s^{-1} at room temperature as a reference and normalises amorphisation data from several sources ([27] for InP, [27,28] for GaP, GaSb and InAs, [29] for GaAs, AlAs and GaN, and (J.S. Williams, unpublished) for InN and AlN). For AlAs, GaN and AlN, dynamic annealing is dominant and amorphisation is extremely difficult to initiate. Only at very high doses for AlAs and GaN is it possible to achieve amorphisation and here the amorphous phase nucleates on a dense network of extended defects [25]. Fig. 3 compares the build up of disorder with increasing implantation dose in these two compounds with that in GaAs for implantation at 77 K [29]. For GaN and AlAs, the amorphous threshold dose is almost three orders of magnitude higher than GaAs, that is every lattice atom has been displaced ~1000 times (1000 dpa). In such cases, it has been suggested [25] that increasing the dose gives rise to an increasing density of extended defects which continually raises the free energy of the system until it is energetically favourable for the system to collapse to the amorphous phase. This idea is consistent with an earlier proposal for amorphisation of Si under specific implantation conditions [30]. Fig. 4 [25] illustrates this process: implantation damage increases the free energy of the crystalline phase until it exceeds that for the amorphous phase. In semiconductors there is a kinetic (energy) barrier to recrystallisation and the amorphous phase is metastable. In metals and some other materials there is practically no barrier to crystallisation and the amorphous phase is not stable even at cryogenic temperatures: in these systems dynamic annealing is extremely efficient and amorphisation is impossible unless the implanted impurity acts to stabilise an amorphous phase [5].

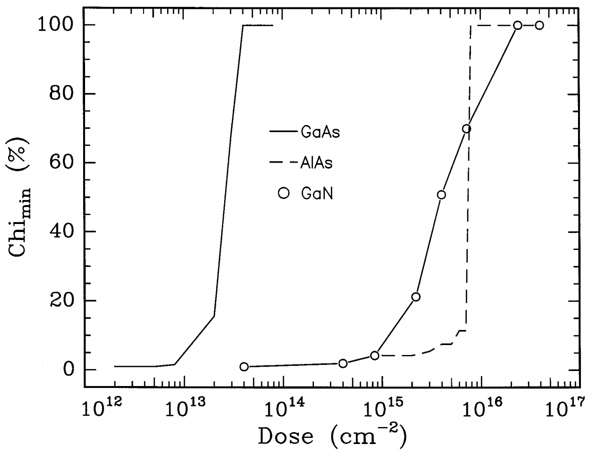

Fig. 3. Normalised minimum channeling yield from ion channeling spectra plotted as a function of dose for three semiconductors showing the damage build up with dose of 90 keV Si ions at 77 K. Taken from [39].

As shown in Fig. 1(b), increasing the implantation temperature increases the dynamic annealing rate until it dominates the damage production rate and amorphisation is eventually suppressed. As the temperature is increased, the transition from amorphous phase production to only defective crystal can be very sharp. This is illustrated by the ion channeling spectra in Fig. 5(a) for GaAs irradiated with Si ions to a dose of 10^{15} cm^{-2} [31]. At 74°C, a buried amorphous layer is formed under these implant conditions but at 80°C the ion channeling spectrum hardly indicates any discernible damage. The peak damage is plotted as a function of temperature in Fig. 5(b) to indicate the sharpness of this transition. Indeed, TEM [32] has shown a continuous amorphous layer at temperatures below 72°C but only a low level of clusters and dislocation loops above 77°C.

Finally, to complete this section, some comments on damage removal during annealing are in order. For silicon, amorphous layers usually crystallise by solid phase epitaxial growth to completely remove the damage and restore the perfect crystal lattice at temperatures ~600°C [33,34]. However, layers that are not amorphous are much more difficult to repair. Preamorphous damage evolves into {311} defects (rodlike clusters of silicon interstitials) at temperatures ~750°C, which break up into small dislocation loops at higher temperatures [35]. Such loops require temperatures above 1000°C to completely remove them [6]. For compound semiconductors, damage removal is more complex and most often more difficult. For example, amorphous GaAs layers do not perfectly recrystallise on annealing but leave behind a highly twinned and defective crystalline layer [36] which repairs at temperatures exceeding 750°C. Other materials such as GaN and SiC, both of which have a high melting point (>2300°C) require annealing temperatures exceeding 1400°C to remove extended defects [37,38]. Indeed, GaN amorphous layers do not recrystallise epitaxially but are polycrystalline following annealing [39]. A general rule of thumb here is that temperatures of ~2/3 of the melting point (K) are needed for removal of extended defects.

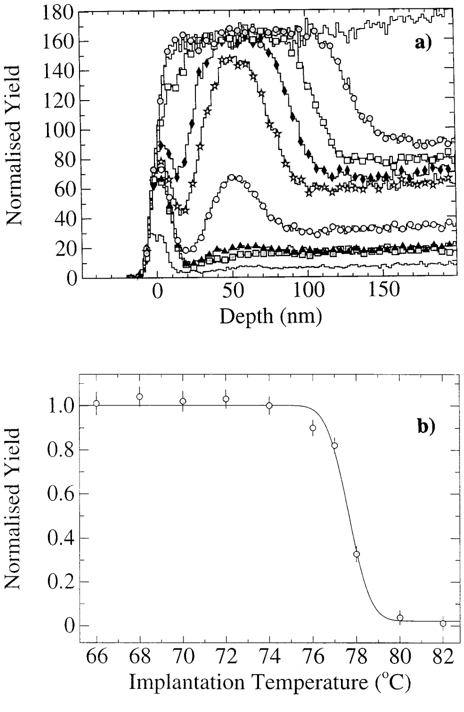

Fig. 5. Ion channeling profiles GaGs showing the damage resulting from implantation of 95 keV, 1×10^{15} Si cm^{-2} at a flux of 4.8×10^{13} cm^{-2} s^{-1} at temperatures of 62°C (shaded circles), 70°C (open squares), 74°C (diamonds), 76° (stars), 78°C (open circles), 80°C (triangles), and 82°C (shaded squares). (b) Normalised yield from (a) plotted as a function of implantation temperature. Taken from [31].

3. Compound formation

The last row in Table 1 lists the typical conditions for compound formation in which the implant concentration exceeds several tens of atomic percent. Typical doses are $>10^{17}$ cm^{-2} and the degree of sputtering of the substrate determines the maximum concentration that can be achieved. Alloys of amorphous GeSi have been achieved by implanting high doses of Ge into silicon [40] and subsequent crystallisation can lead to crystalline alloys. In other cases chemical driving forces can lead to compound formation directly during implantation. Formation of buried and continuous SiO_2 layers (the so called SIMOX process) is one such case which is now an accepted industry process for forming buried insulating layers in silicon circuits [41]. Silicides can also be formed by high dose implantation of metals or ion beam mixing of metal films on silicon [12,42,43] and, if the conditions are suitable, buried epitaxial silicides (typically $NiSi_2$ and $CoSi_2$) can form [44]. For immiscible systems, such as when high doses of Sb are implanted into Si [45], precipitation can occur during bombardment, indicating that the system is driven towards thermodynamic equilibrium.

The non-equilibrium aspects of ion implantation, composition limits imposed by sputtering and thermodynamic driving forces for compound formation are interesting to consider in high dose implantation. Some of these issues are illustrated in Fig. 6 for the case of oxygen bombardment of silicon [46]. For normal incidence bombardment of silicon with 15 keV O^+ ions at 77 K, the ion channeling spectra in Fig. 6(a) show that the composition builds up to SiO_2 with increasing dose. Once this composition is reached, oxygen appears to be mobile in SiO_2 under continued bombardment and a continuous layer is formed with quite a sharp boundary between Si and SiO_2. These data indicate that strong chemical driving forces exist for SiO_2 formation under ion bombardment even at 77 K. Fig. 6(b) shows the effect of angle of beam incidence on the composition of the film [46]. Note that SiO_2 is only formed under bombardment conditions where the incident beam is less than 30° from normal incidence: at larger angles enhanced sputtering does not allow the composition to reach SiO_2.

4. Diffusion and gettering

As mentioned previously, two crucial issues in advanced silicon device processing are the need to remove trace amounts of metal contaminants from active device regions and transient enhanced diffusion of dopants during low temperature annealing. In both of these areas, ion implantation has an important role to play. In the former case, implantation can be used to

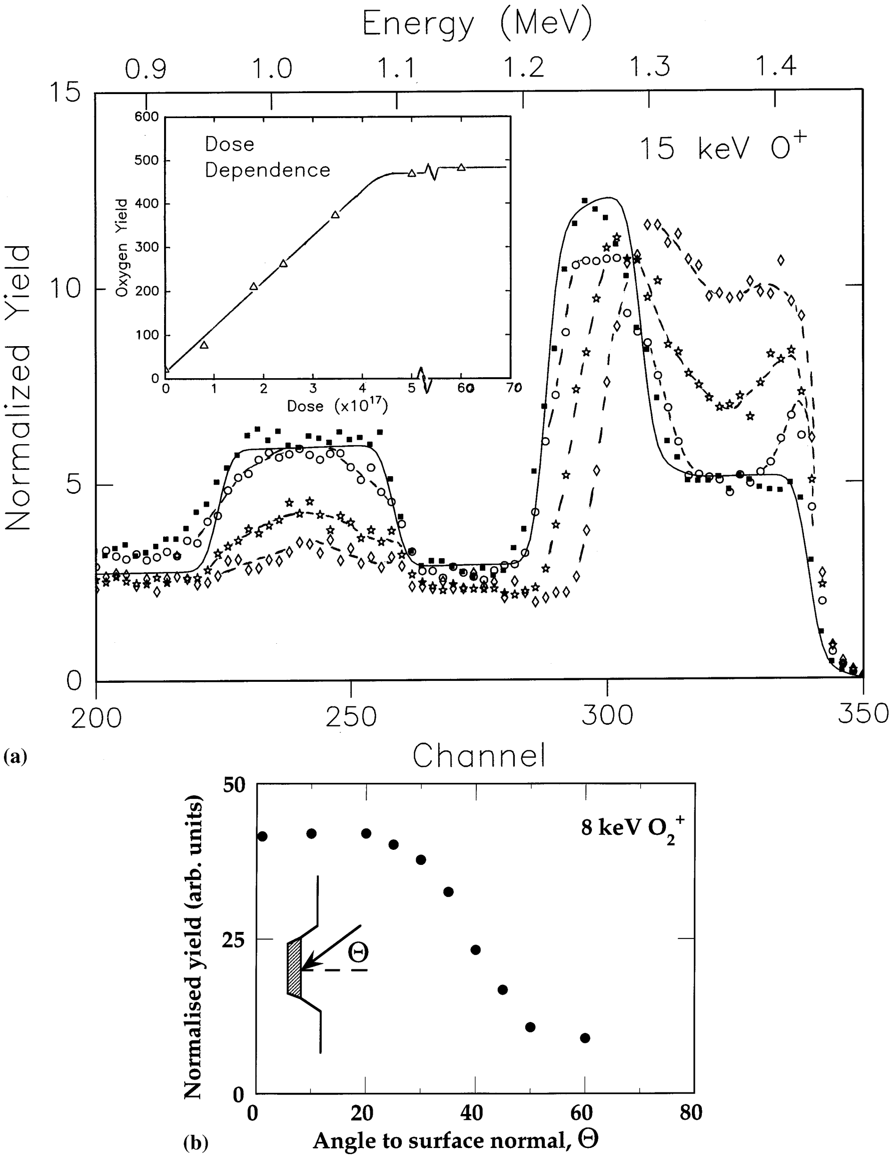

Fig. 6. (a) Ion channeling spectra for increasing doses of 15 keV O ions at 0° beam incidence (0.8, 2.3, 3.5, and 6 × 10^{17} cm^{-2}). The inset shows the increase in O yield with increasing dose. (b) The oxygen yield as a function of angle of beam incidence showing the drop in O yield from SiO_2 stoichiometry at angles greater than ~30°. Taken from [46].

generate a layer of damage away from active devices and this layer can trap metals during subsequent annealing. This so called proximity gettering approach [47] has been quite successful in improving device performance [48]. Recently, implantation of either He [49] or H [50] ions into silicon has been used to introduce a band of cavities at a precise depth and these cavities used as an efficient getter layer for metals in silicon. An example of cavity gettering is shown in Fig. 7 [51]. In this case, a band of cavities was first introduced into silicon at a depth of 1 μm by implantation of 100 keV H ions to a dose of 3×10^{16} cm^{-2}, followed by annealing at 850°C for 30 min. Au was then implanted into the near-surface at 95 keV to a dose of 8×10^{14} cm^{-2}. The upper trace in Fig. 7 shows the as-implanted Au profile (from Rutherford backscattering data) and the lower trace shows the Au redistribution to the cavity band following a subsequent annealing at 850°C for 1 h. The TEM cross-sectional micrograph in the lower panel of Fig. 7 shows the well formed cavity band. Au is observed to decorate the cavity walls but also to form precipitates within the cavities [52]. The efficient gettering example in Fig. 7 illustrates the non-equilibrium aspect of implantation. When the Au is implanted into silicon, the peak concentration exceeds the maximum solubility of Au in silicon by several orders of magnitude [53]. During annealing at 850°C, the Au is mobile and diffuses interstitially [54]. There is a strong driving force for precipitation of Au and, since the cavities are strong sinks for interstitial Au, diffusing Au preferentially segregates at cavities [52].

The second area of current concern for advanced silicon devices, that of transient enhanced diffusion (TED) of dopants, is thought to be mediated by silicon interstitials which are a result of implantation damage [35]. An example of TED of B-implanted silicon is shown in Fig. 8 [55]. The as-implanted B profile broadens considerably when it is annealed at 850°C for 1 h. This occurs as a result of the release of silicon interstitials from {311} defects during annealing: mobile interstitials kick out substitutional B atoms which then rapidly diffuse interstitially [35]. In Fig. 8, the effect of a cavity band on TED of boron is also shown. TED is suppressed in the vicinity of the cavities as a result of loss of silicon interstitials which are gettered to cavities [55].

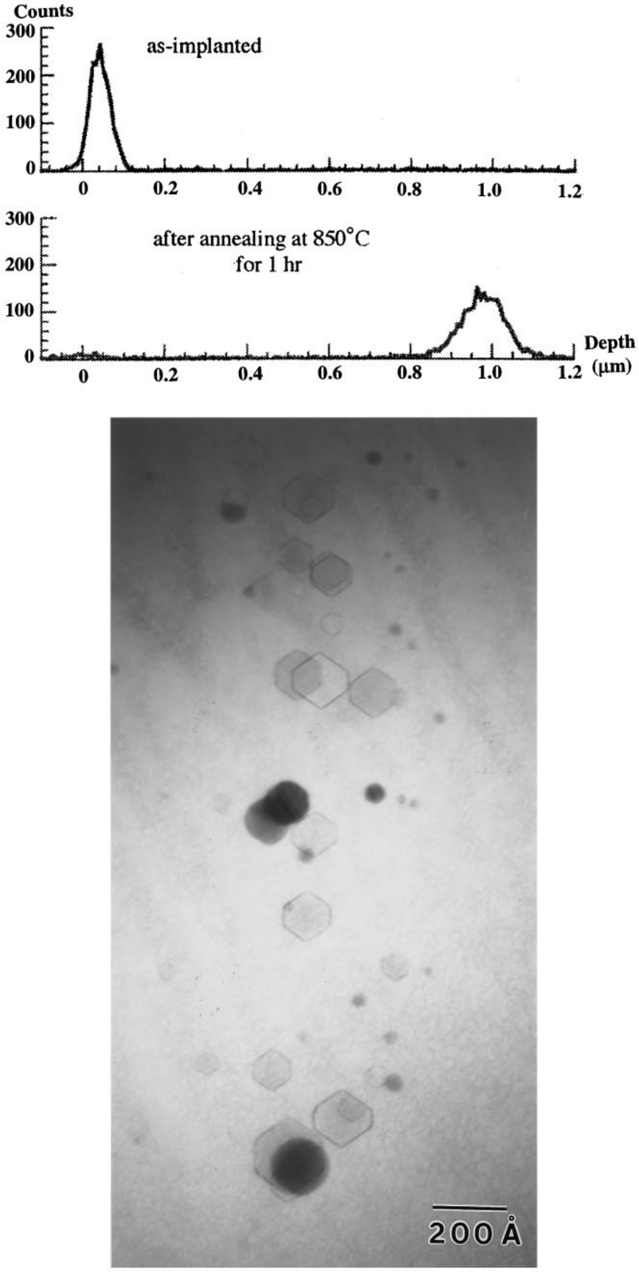

Fig. 7. Au profiles from RBS spectra showing the redistribution of Au from the implanted surface region to a band of cavities at 1 μm during 850°C annealing. An XTEM micrograph in the lower part of the figure shows Au decoration of cavities. Taken from [51].

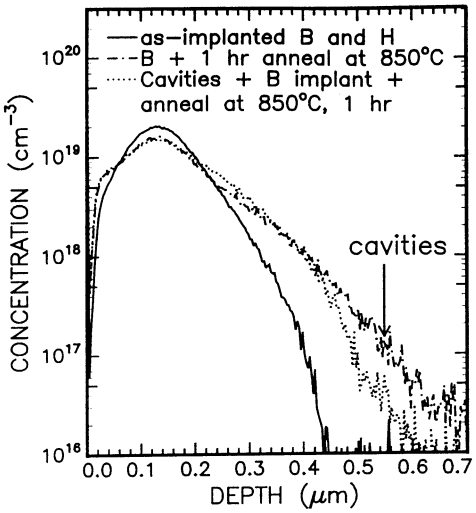

Fig. 8. Secondary ion mass spectrometry profiles showing the effect of cavities on the TED of B in Si. Taken from [55].

5. Some further applications of implantation

Figs. 9 and 10 show some further applications in compound semiconductor devices where ion implantation damage is used to advantage. In Fig. 9, a schematic of a heterostructure bipolar transistor (HBT) is shown [56]. There are two applications where implantation damage is used to improve the performance of such devices: (i) to electrically isolate one transistor from the next by rendering the structure highly resistive between adjacent devices; and (ii) to selectively damage the collector region to reduce the base-collector capacitance. In the first case, several keV energy implants of H^+ or O^+ are needed to adequately damage the entire several microns of the structure [57] or, alternatively, a single MeV implant of say 5 MeV O^+ can be used [56]. In the latter case, the MeV ions create roughly uniform damage over several microns and the damage only increases substantially much deeper in the substrate. By carefully adjusting the dose it is possible to remove the active carriers from the active part of the structure to generate a layer of high resistance. In the second case the dose is much lower to just remove the carriers from the low carrier concentration collector region without significantly altering the conduction in the adjacent higher doped layers. Both these implantation schemes have been successfully used to substantially improve device performance [56].

A second application is shown in Fig. 10, where H-implantation has been used to shift the wavelength

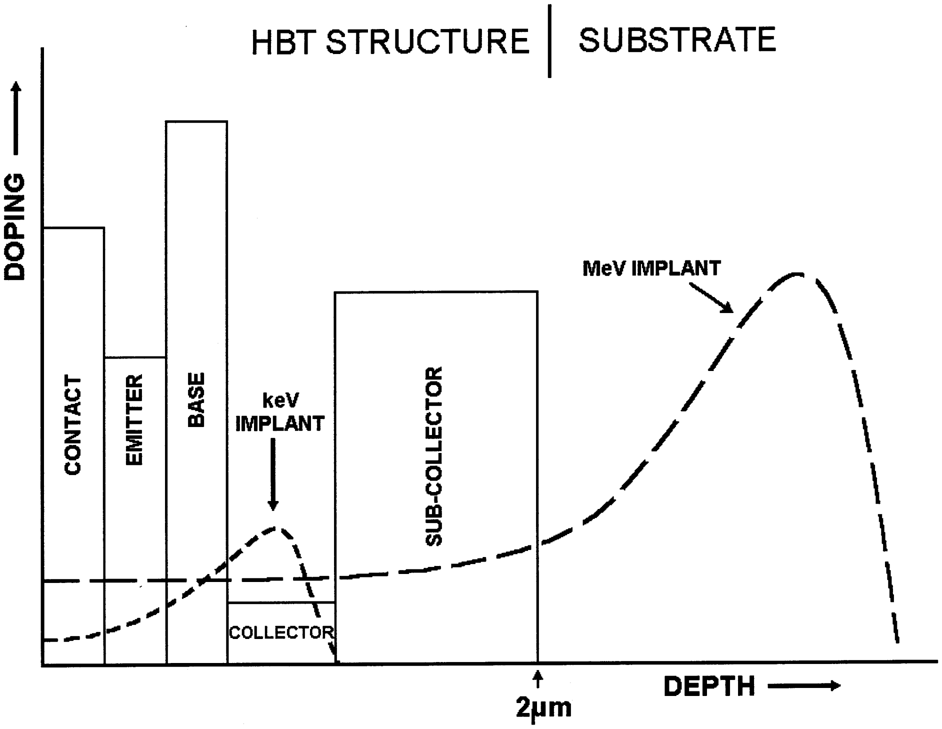

Fig. 9. Schematic showing the use of keV and MeV implants to isolate devices and reduce base-collector capacitance. Taken from [56].

of light emission from multiple quantum well (MQW) structures in GaAs/AlGaAs multilayers [58]. The example shows four quantum wells of different thickness (which results in different emission wavelengths) and a dose of 5×10^{15} H cm^{-2} has been used to disorder and slightly intermix the adjacent AlGaAs/GaAs layers to achieve the desired blue shift of the emitted light in each of the quantum wells. This particular process can be used to tune the wavelength of individual lasers on a single chip [58,59].

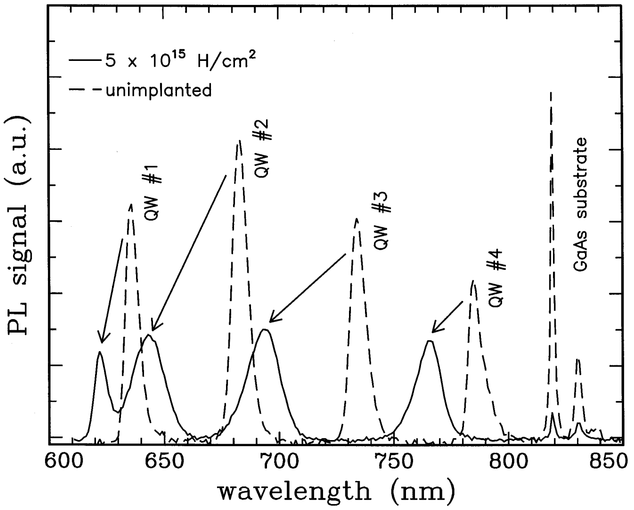

Fig. 10. Low temperature photoluminescence spectra for a MQW sample showing the effect of H-implantation on emission wavelength. Taken from [58].

6. Conclusion

It has been shown that ion beam modification of semiconductors is an indispensable process for the production of devices and circuits. The needs of the semiconductor industry have been the major driving force for fundamental ion beam research in semiconductors and for the development of new ion beam applications. Damage production and its removal have been shown to be major issues which have stimulated an enormous body of literature over 3 decades. High dose implantation has also been used for forming both insulating compounds and conducting layers in devices. Removal of metals from active device regions and reducing TED of dopants are two of the key technological issues which have been successfully addressed by implantation processes. Finally, it was also shown that controlled introduction of ion damage into devices can often improve device performance and desirably alter device properties.

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