ION IMPLANTATION IN SEMICONDUCTORS

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ABSTRACT

Ion implantation is being applied extensively to silicon device technology. Two principle features are utilized: 1) charge control in MOS structures for threshold shift, autoregistration, and complementary wells and 2) distribution control in microwave and bipolar structures. Another feature that has not been extensively exploited is to combine the advantages of the high resolution capabilities of electric beam pattern delineation with the low lateral spread inherent in the implantation process. This talk reviews some of the general features of the characteristics of implanted layers in terms of depth distribution, radiation damage and electron activity. Implantation processes in silicon are reasonably well understood. There remain areas which require further clarification. For compound semiconductors, particularly GaAs, implantation techniques offer attractive possibilities for the fabrication of high frequency devices. In these materials, the substrate temperature during implantation and the dielectric coating required to prevent dissociation during thermal anneal play major roles.

INTRODUCTION

Ion implantation is the introduction of atoms into a solid substrate by bombardment with ions in the keV to MeV energy range. The basic concepts of implantation processes have been treated in conferences and books (1-4). It was early recognized that this technique provides the possibility of introducing a wide selection of atomic species and also external control of both the number of atoms per cm^2 introduced into the semiconductor and the depth distribution of the implanted species. This is in contrast to diffusion processes where temperature governs the surface concentration and time and temperature determine the depth distribution.

The initial impact on silicon technology was in charge control. It has been possible to control the number of dopant atoms per cm^2 to about 1% over the surface of a wafer, and to control the number within 3% from wafer to wafer. This in combination with the fact that simple masking techniques can be used to define the geometrical area of the implanted region led to extensive applications to MOS technology (5). An extension of this work has led to the use of electron beams to expose photoresist so that one micron gate lengths can be fabricated for N-channel enhancement-depletion mode FET's (6).

The distribution control inherent in the implantation process has been utilized in fabricating IMPATT type devices (7,8). Here multiple implantations are performed at different energies and ion doses to achieve the desired dopant profile.

There are limitations to the implantation process. At energies $\lesssim$ 300 keV, the range of the implanted ion is typically less than one micron and often of the order of a few tenths of microns. Diffusion steps are necessary to achieve greater depths. Lattice disorder and radiation damage induced defects are caused by the implanted atom as it comes to rest in the semiconductor. Although implantation is considered as a room temperature process, it is necessary to thermally anneal the samples after implantation. Often these anneal temperatures are comparable to those used in diffusion.

IMPLANTATION IN SILICON

Silicon provides an ideal host for studying the basic parameters and concepts involved in the implantation process. The parameters are: substrate temperature during implantation, anneal temperature, total dose of ions per cm^2 and dose rate, beam energy and beam species. All of these parameters should be considered when evaluating implantation behavior in any semiconductor. For silicon boron, phosphorus and, more recently, arsenic are generally implanted at room temperature and annealed to about 900°C to achieve the maximum electrical activity. Where aluminum metallization is employed prior to implantation, anneal temperatures around 550°C are used with some loss in dopant efficiency.

Range Distributions

If channeling effects are negligible the depth distribution of implanted ions is roughly Gaussian and can be characterized by a mean projected range R_p and a standard deviation ΔR_p about the mean (4). Approximations and rules of thumb have been given by Schiøtt (9) and tabulations by Johnson and Gibbons (10). These provide reasonable estimates for the projected range (11). In most cases there is no major change in the peak of the distribution following anneal at 900°C (12). However, the width of the

profile is generally broader than predicted and there are often tails in the distribution. In device applications where the depth distribution is important, it is generally necessary to make an experimental determination of the depth profile.

The crystalline rows and planes can steer or "channel" the implanted ions significantly deeper into the crystal than in amorphous targets (4). Channeled distributions for arsenic (13) and phosphorus (14,15) implantations have been measured by C-V techniques. The maximum range to which the ions penetrate is determined by the incident energy and orientation of the silicon and can be a factor of ten deeper than the projected range R_p for incidence away from any major crystal axis. Conditions are very stringent for the incident ion to remain channeled throughout its trajectory. The shape of the depth distribution is strongly influenced by lattice disorder, by the amount of oxide layer on the surface, and by any misorientation between the incident ion beam and crystal axis (14,15). Because of the stringent conditions required to obtain well-behaved channeling distributions, there are serious limitations on the use of this technique in general fabrication steps.

Lattice Disorder and Radiation Damage

Over the past three or four years one of the major efforts has been to characterize the amount and the nature of lattice disorder produced by energetic ions (1-4). The amount of lattice disorder depends on ion mass and energy, substrate temperature during implantation, dose rate, and dose. It is a fascinating and complex field.

Some simple approximations can be made. For low dose ($\approx 10^{12}/cm^2$) implantations, there are strong correlations in defect species between ion implanted and fast neutron irradiated silicon (16). Most of the gross disorder anneals out at temperatures around 300°C but higher temperatures are required to remove the compensating defects. At higher ion doses (10^{14} - $10^{15}/cm^2$) an amorphous layer is formed (4). During anneal at temperatures of about 550°C, this amorphous layer recrystallizes epitaxially on the underlying crystalline material. There are a significant number of defects in the recrystallized layer (17). The lifetime of minority carriers is very sensitive to the presence of defects. With increasing ion dose, higher anneal temperatures ($\gtrsim$ 900°C) are required to recover carrier lifetimes (18).

In general, then, it is desirable to use as high an anneal temperature as possible to remove radiation induced defects. Temperatures of 900 to 950°C are commonly employed. With low dose implants typical of MOS technology temperatures below 550°C can be employed.

Lattice Location and Electrical Behavior

Following implantation and anneal, n-type (Group V) dopants occupy substitutional sites. The behavior of Group III elements is much more complex (4). Boron, for example, has been found to move off substitutional sites during anneal and temperatures of about 900°C are required to obtain a high substitutional fraction (4).

Perhaps the most thoroughly investigated aspect of ion implantation in silicon is the electrical behavior of the implanted layer. In general, Hall effect measurements in combination with layer removal techniques have been made. The number of carriers per cm^2 is determined as a function of anneal temperature for various doses of implanted ions (1-4).

A rough rule is that after anneal at temperatures of 900°C to remove radiation damage defects, all the implanted dopant atoms become electrically active (4). This behavior (except for arsenic) holds for cases where the concentration of the implanted species is less than the equilibrium solubility at the anneal temperature. For arsenic, the maximum concentration of electrons is about $10^{20}/cm^3$, a value well below the maximum substitutional concentration. In cases where an amorphous layer is formed, there is a pronounced anneal stage at 550°C. This fact is often utilized to obtain high electrical activity at low anneal temperatures (19).

IMPLANTATION IN GaAs

The natural extension of the work in silicon is to investigate implantation processes in compound semiconductors. For these materials, diffusion technology is at a rather primitive level as compared to silicon, so that implantation would not have to compete with a well established technology. In addition, the higher electron mobility in GaAs, for example, lends itself to high frequency device concepts.

The major constraint is that compound semiconductors tend to dissociate when annealed to the temperatures required to remove damage induced defects. The simplest method of avoiding this dissociation is to encapsulate the implanted samples with a dielectric coating. Some of the initial efforts in the evaluation of implanted layers in GaAs were to determine if good electrical activity could be obtained without encapsulation of the layer (20). This approach was not successful.

Anneal temperatures of 800 to 900°C are generally required to obtain the maximum number of carriers per cm^2 in the implanted layers (21). These anneal temperatures and encapsulation with SiO_2 are generally sufficient to achieve good electrical activity for p-type dopants. The carrier concentrations in the implanted layer are close to the solubility level.

The initial results obtained on implanted layers in GaAs for n-type dopants were disappointing in that very low electrical activity was found (22). More recently it has been observed that good electrical activity can be obtained by proper choice of the implantation temperature and encapsulating layer (23). In this case silicon nitride was used as the encapsulating layer to

prevent out-diffusion of Ga and substrate temperatures of 150 to 300°C were used to reduce the residual disorder. The maximum concentration of electrons was comparable to that obtained by doping GaAs with Te during crystal growth.

The results from studies of implantation of p- and n- type dopants in GaAs indicate that good electrical activity can be obtained. Rather high anneal temperatures of 800-900°C and encapsulating layers are required. In spite of these difficulties, one can now anticipate use of implantation in GaAs device applications.

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