1 Fundamentals

1.1 Field-effect transistors

1.1.1 General layout

A transistor is an electronic semiconductor device for switching or amplifying electricity. The current can flow through two junctions - called drain and source -, while the third (gate electrode) is used for control. In addition to the field-effect transistor (FET) which is described here, there is another basic transistor, the bipolar transistor. The operation of the bipolar transistor is based on charge carriers of both polarities (thus bipolar), holes and electrons. Field-effect transistors, also known as unipolar transistors, use either electrons or holes for the transport of electricity.

The transistor is the basic component in semiconductor manufacturing, in modern microchips there are found several millions to billions of transistors. Through the combination of multiple transistors, all logic gates can be implemented in order to obtain logic output signals of corresponding input signals. Thus transistors form the heart of every microprocessor, memory chip, etc. The transistor is the most abundant object made by mankind, and thus became indispensable in today's life.

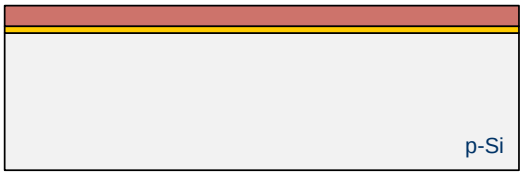
The transistor is built up layer by layer. This article describes the basic structure of a simple field-effect transistor, the various possibilities to realize the miscellaneous layers will follow in the later chapters.

1.1.2 Construction of a n-channel FET

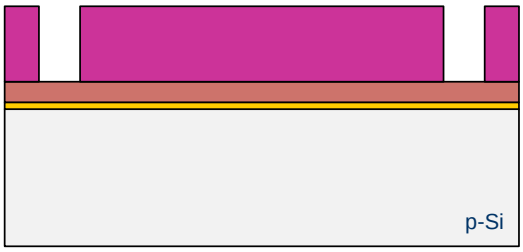
1. Substrate: Basis for a n-channel field-effect transistor is a p-doped (boron) silicon substrate.

2. Oxidation: On top of the substrate, a thin layer of silicon dioxide SiO_2 (the gate oxide) is created via thermal oxidation. It is used for insulation of the later deposited gate and the substrate.

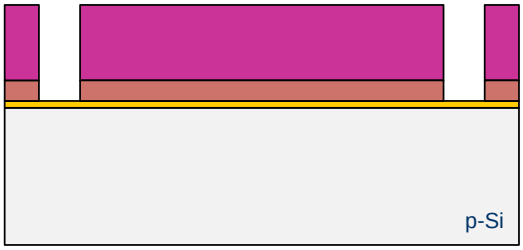
3. Deposition: In a LPCVD process nitride is deposited, it is used later as an masking during the field oxidation.



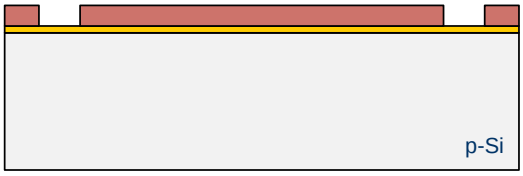
4. Photolithography: On top of the nitride a photoresist is spun on, exposed and developed. Thus a structured coating layer is fabricated which serves as an etching mask.



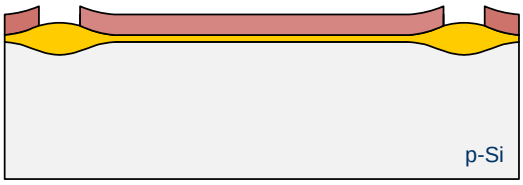
5. Etching: Only at resist free sites nitride is removed using reactive ion etching.



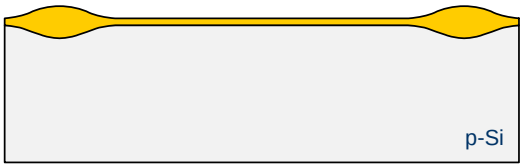
6. Resist removal: Subsequent the resist mask is removed in a wet-chemical developer solution.



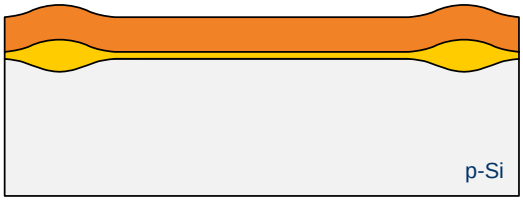
7. Oxidation: During field oxidation, the nitride serves as a mask layer, the thermal wet oxidation takes place only on the bare gate oxide. The grown field oxide is used for lateral isolation to adjacent devices.



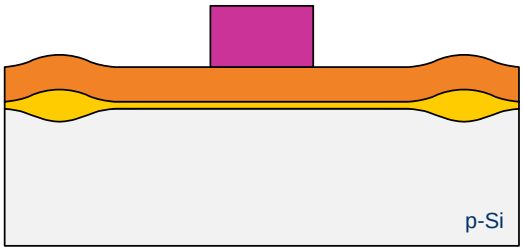
8. Etching: Subseuqent to the oxidation, the nitride is removed in a wet chemical etching process.



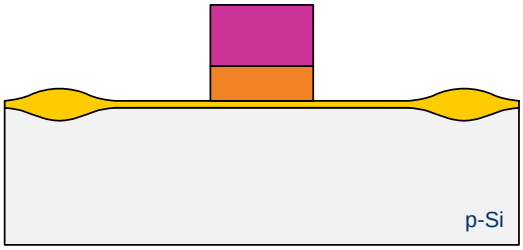
9. Deposition: Via low pressure CVD, polycrystalline silicon is deposited which represents the gate electrode.



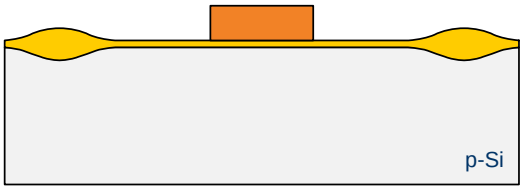
10. Photolithography: Again a resist layer on top of the polysilicon is patterned.



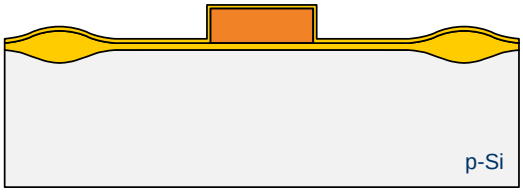
11. Etching: The photoresist in turn serves as a mask layer, via reactive ion etching the gate is patterned.



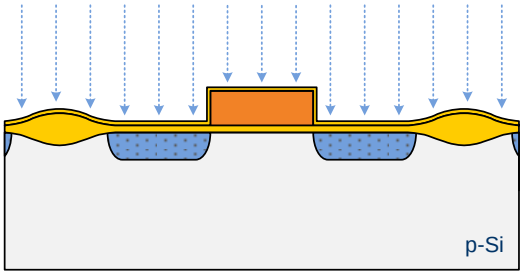
12. Resist removal: The resist is removed via wet-chemical etching.



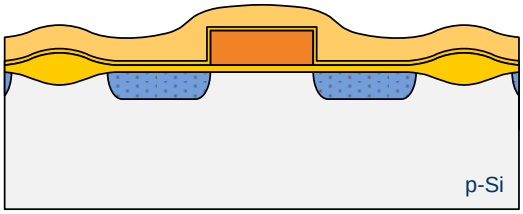
13. Oxidation: A thin oxide (post oxide) is deposited as an insulating layer for the gate electrode as well as a spacer for the subsequent source and drain implantation.



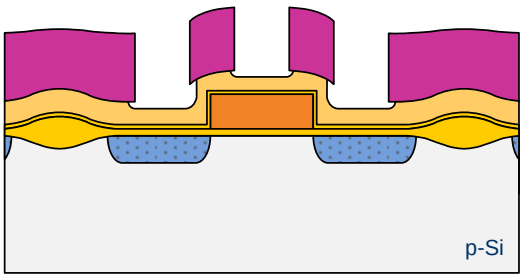
14. Ion implantation: Via ion implantation with phosphorus, the source and drain regions are introduced (n-type). Since the gate electrode acts as an mask during implantation, the width of the n-channel between the source and drain is preset. This is called self alignment.



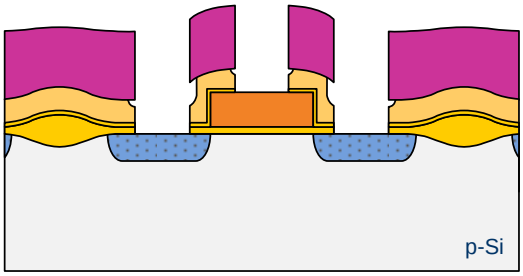
15. Oxidation: As an isolation a nonmetal is deposited (e.g. oxide). This happens in a LPCVD process with TEOS, which provides a good step coverage.



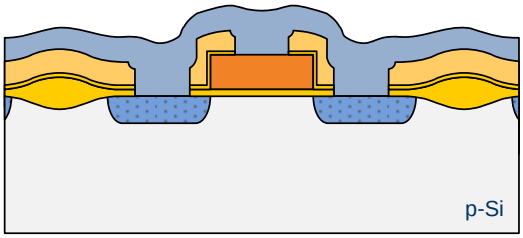
16. Photolithography and etching: In a further step a resist layer is structured and the edges of the contact holes are rounded in an isotropic etch process.



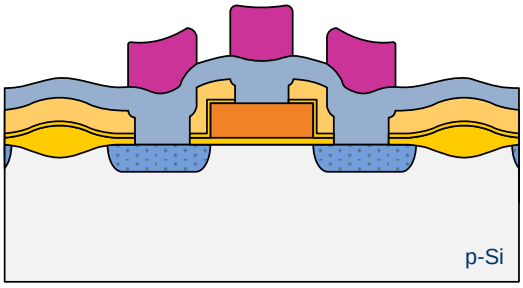
17. Etching: Subsequently the contact holes are opened in a highly anisotropic etch process.



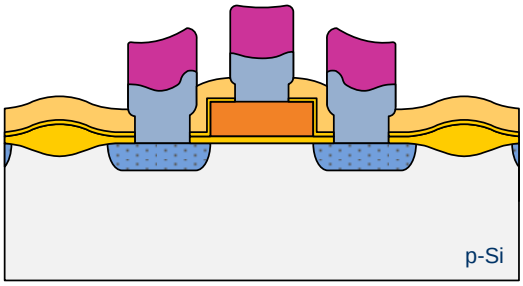
18. Metallization: The contact holes are filled with aluminum via sputtering.



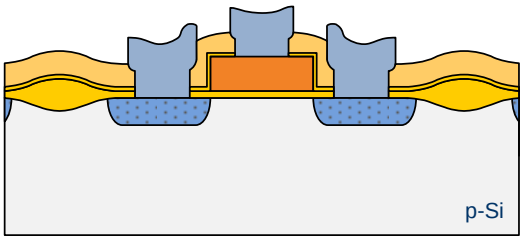
19. Photolithography: In a final lithography step a new resist mask is patterned.



20. Etching: The pattern is transferred into the underlying metallization in an anisotropic dry etch process.



21. Resist removal: Finally, the resist is removed and aluminum conductors remain to actuate the transistor.



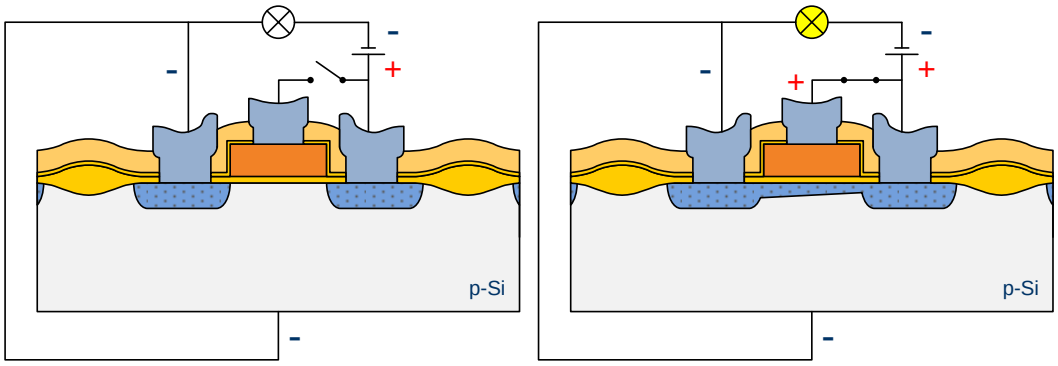
Actual the construction of a transistor is much more complex, since additional planarization layers for photolithography are neccessary or secondary drain and source implantations have to be done to adjust the threshold voltage accurately. On the slopes of the gate elektrode additional (side wall) spacers can be formed to set the exact length of the channel or fine tune the doping profile respectively.

1.1.3 Mode of operation

Enhancement-mode:
Without a positive voltage applied to the gate there are no electrons available, which could act as free charge carriers between source and drain, since the substrate is p-doped. In steady state holes in the substrate act as majority charge carriers, while the electrons are minority charge carriers.

A positive voltage applied to the gate attracts electrons in the substrate, while holes are pushed away. Thus forming a conducting n-channel beneath the gate electrode and in-between source and drain, respectively. The insulating silicon dioxide layer prevents a current flow between the substrate and the gate.

Since the transistor blocks the current flow without an applied voltage, the transistor is also called self-locking.



(a) (b)

Fig. 1.1: Enhancement nFET

Depletion-mode:
With a light n-type doping between the source and drain, a conductivity is even possible without a gate voltage (a voltage between source and drain is sufficient). So-called depletion FETs, or self-conducting transistors block the current flow only, if the voltage applied to the gate electrode is lower than the voltage at the source port. If the gate voltage is decreased, the electrons that are located beneath the gate, are pushed away - the conductive electron-channel is lost.